REMARKS

In the instant amendment, claims 1-11 and 25 are cancelled, without prejudiced, as being directed to a non-elected group. Applicants, of course, reserve the right to file these claims in a divisional application. Claims 12-24 and 26 are submitted for further examination.

Applicants acknowledge the Draftsperson's objection set forth on Form PTO-948 and directed to the top margins of FIGS. 1, 3 and 5. Corrected figures are submitted herewith to obviate this objection to the drawings. Applicants appreciate the Examiner's acknowledgement of applicants' claim for foreign priority and the receipt of a certified copy of the priority document.

Reconsideration of the rejections in this application is respectfully requested.

Procedural Summary

In the outstanding Office Action of February 28, 2001, the Examiner rejected claims 20 and 22 under 35 U.S.C. § 112, first paragraph, because the specification, while being enabling for the elements (i) and (ii), does not reasonably provide enablement for (iii). The Examiner rejected claims 12-16, 18-22, 24 and 26 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,166,423 to Gambino et al. ("the Gambino et al. reference") in view of United States Patent No. 5,498,889 to Hayden ("the Hayden reference"). The Examiner also rejected claims 14 and 17 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Hayden reference further in view of United States Patent No. 6,074,907 to Oh et al. ("the Oh et al. reference"). The Examiner further rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Hayden reference further in view of United States Patent No. 6,066,555 to Nulty et al. ("the Nulty et al. reference").

A. Asserted Rejection Under 35 U.S.C. § 112, first paragraph

The Examiner rejected claims 20 and 22 under 35 U.S.C. § 112, first paragraph, because the specification, while being enabling for the elements (i) and (ii), does not reasonably provide enablement for (iii). Although applicants respectfully traverse this rejection, applicants amended claims 20 and 22 to clarify element (iii). Accordingly, applicants respectfully submit that this rejection has been obviated and requests withdrawal of this rejection.

B. Asserted Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 12-16, 18-22, 24 and 26 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,166,423 to Gambino et al. ("the Gambino et al. reference") in view of United States Patent No. 5,498,889 to Hayden ("the Hayden reference"). The Examiner also rejected claims 14 and 17 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Hayden reference further in view of United States Patent No. 6,074,907 to Oh et al. ("the Oh et al. reference"). The Examiner further rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Hayden reference further in view of United States Patent No. 6,066,555 to Nulty et al. ("the Nulty et al. reference").

1. Asserted Obviousness - Claims 12-16, 18-22, 24 and 26

In the initial obviousness rejection, the Examiner rejected claims 12-16, 18-22, 24 and 26 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,166,423 to Gambino et al. ("the Gambino et al. reference") in view of United States Patent No. 5,498,889 to

Hayden ("the Hayden reference"). In view of the significant technical distinctions between the present invention and the cited prior art references, applicants respectfully request reconsideration and withdrawal of this rejection.

At least one patentably distinct feature of the present invention is related to the structure of and use of a conducting sidewall spacer 208 to prevent the inferior disconnection problem on lower edges of the first via hole h1. This disconnection problem of conventional capacitors is illustrated in Fig. 5 of the present invention by broken circles marked by letter 'A.'

The Examiner cited the combination of the Gambino et al. reference and the Hayden reference as follows:

> With regard to claim 12, Gambino et al. discloses in figure 11 providing an insulating substrate (305). Gambino et al. discloses in figure 11 simultaneously forming a first wire line (315) and a lower electrode (310) on predetermined surfaces of the insulating substrate. Gambino et al. discloses in figure 11 forming an interlevel insulating layer (307) on the substrate, on the first wire line, and on the lower electrode. Gambino et al. discloses in figure 12 selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole (320) having sidewalls and disposed above the lower electrode; and (ii) a second via hole (330) disposed above the first wire line. Gambino et al. discloses in figure 13 forming a conductive layer (328) on the interlevel insulating layer and in the first and second via holes. Gambino et al. discloses in figure 14 etching back conductive layer to form: (ii) a conductive plug in the second via hole; and (iii) an exposed surface containing the conductive plug, the predetermined surface of the lower electrode, and the predetermined surfaces of the interlevel insulating layer. Gambino et al [sic] discloses in figure 15 forming a dielectric layer on the exposed surface. Gambino et al. discloses in figure 16 removing (332 and 334) the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on a predetermined surface of the lower electrode. Gambino discloses in figures 17 - 18

> simultaneously forming: (i) a second wire line (324) connected to the conductive plug; and (ii) an upper electrode (324) connected to the dielectric layer. Gambino et al. does not disclose etching back the conductive layer to form: (i) a spacer on the sidewalls of the first via hole. Hayden teaches in figure 4 etching back a conductive layer to form: (i) a spacer (32) on the sidewalls of a first via hole (30). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conductive spacers of Hayden in the first via hole of Gambino et al. in order to maximize the area of the capacitor as stated by Hayden in column 4, lines 28 - 30. Once the conductive spacers were formed in the first via hole of Gambino et al. it is obvious that the exposed surface would contain the spacer, and the dielectric layer would remain disposed on a predetermined portion of the spacer.

Office Action of Feb. 28, 2001, at pp. 3-4.

As recited above, the Examiner indicated that the conductive spacers of the Hayden reference could have been used "in the first via hole of Gambino et al. in order to maximize the area of the capacitor as stated by Hayden in column 4, lines 28 - 30." In the present invention, however, conductive sidewall spacers are not intended to maximize the area of the capacitor. While the Hayden reference, at column 4, lines 28-30, does teach using the sidewall spacers for maximizing the area of the capacitance, the present invention teaches that the sidewall spacers of the present invention are intended to prevent the dielectric disconnection problem as illustrated in Fig. 5. In addition, there are several structural differences in the sidewall conductive spacers of the Hayden reference and the present invention.

First, in the present invention, the conductive sidewall spacer 208 is formed directly on the flat horizontal conducting layer, 202a (see Fig. 10). Thus, in the present invention, the sidewall spacer 208 and the flat horizontal layer 202a, together constitute the bottom plate of the MIM capacitor. In the Hayden reference, the conducting sidewall spacer 32 is not touching the

flat horizontal conducting layer 18 (see Fig. 6). In fact, the spacer 32 and the horizontal layer 18 are separated by an insulating layer 20, which is a silicon nitride layer, as mentioned at column 3, line 10. In the Hayden reference, the horizontal layer 18 is touching the conducting upper electrode layer 38 (see Fig. 7), whereas, the sidewall spacer 32 alone forms the second conducting plate of the MIM capacitor with conducting layer 26 providing an electrical connection to the sidewall spacer. Thus, in the Hayden reference, the conductive sidewall spacer alone is intended to provide a vertical conductive capacitor plate.

Second, the capacitor dielectric of the Hayden reference is almost entirely formed on the vertical sidewalls of the via hole 30, whereas, in the present invention it is formed on both the vertical sidewalls and the horizontal conducting layer 202a.

Third, in the present invention, top and horizontal conducting layers (214a and 202a, respectively) are separated by the capacitor dielectric layer 212, which overlays the sidewall spacers. In the Hayden reference, however, the top conducting layer 38 and horizontal layer are electrically connected.

As stated above, in the invention, the sidewall spacer is intended to prevent dielectric disconnection problem (as indicated by letter 'A' in Fig. 5) but not to increase the area of the capacitor. However, the MIM capacitor structure of the present invention also provides a high capacitor area while solving the dielectric disconnection problem. In the Hayden reference, the structure of the capacitor is different from that of the present invention and the dielectric disconnection problem solved by the present invention does not exist in that structure.

In view of the differences in structure as well as the difference in purpose related to the sidewall spacers, applicants respectfully submit that the above combination of prior art references is improper to reject any claim in the subject application.

2. Asserted Obviousness - Claims 14 and 17

Another rejection presented by the Examiner rejects claims 14 and 17 under 35 U.S.C. § 103(a) as being unpatentable over the combination of the Gambino et al. and the Hayden references further in view of United States Patent No. 6,074,907 to Oh et al. ("the Oh et al. reference"). The Oh et al. reference is cited for the additional teaching of:

> a dielectric layer that has a structure selected from: (i) a single-level structure containing an oxide layer or nitride layer; or (ii) a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers and mixtures thereof. Oh et al. teaches the multi-level structure is an oxide/nitride/oxide layer (ONO).

The Oh et al. reference at col. 4, lines 49-51.

In view of the significant technical distinctions between the combination of the Gambino et al. and Hayden references and the present invention related to the sidewall spacer 208 of the present invention described above, applicants respectfully traverse this rejection and submit that it should be withdrawn.

3. Asserted Obviousness - Claim 23

The Examiner further rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over the Gambino et al. reference and the Hayden reference further in view of United States Patent No. 6,066,555 to Nulty et al. ("the Nulty et al. reference"). The Nulty et al. reference is cited for the additional teaching of, "sputter etching an interlevel insulating layer and via holes." *The Nulty et al. reference at col. 2, lines 56-60.*

In view of the significant technical distinctions between the combination of the Gambino et al. and Hayden references and the present invention related to the sidewall spacer 208 of the present invention described above, applicants respectfully traverse this rejection and submit that it should be withdrawn.

Conclusion

Since none of the prior art cited, alone or in combination, either anticipates or renders obvious claims 12-24 and 26, it is submitted that these claims are in condition for allowance and notice to that effect is respectfully requested.

Finally, if the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner should not hesitate to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

In view of the foregoing amendments and remarks, reconsideration of this application is respectfully requested, and an early and favorable action upon all the claims is hereby requested.

Respectfully submitted,

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